REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-13 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al. (U.S. Patent No. 5,846,863). Applicant respectfully traverses.

Claim 1 recites that a source slot and a drain contact region are formed at opposite ends of a NAND string disposed on a substrate of the memory array using a single mask, the NAND string comprising a plurality of memory cells connected in series between a source select gate and a drain select gate, where a portion of the drain contact region is formed directly over the drain select gate and where the single mask defines areas for exposing the substrate. This means that the source slot and drain contact region are formed after the formation of the NAND string, source select gate, and drain select gate. There is no indication in Lee et al. of forming a source slot and a drain contact region after the formation of a NAND string comprising a plurality of memory cells, a source select gate, and a drain select gate. Lee et al. shows forming a second gate electrode 114 in spaces between spacers 110 formed in contact with first gate electrodes 106 (Figures 15B, 21B, and 23B). Figures 15 and 15C and column 8, lines 6-8, indicate that the second gate electrode 114 is a word line, suggesting that the second gate electrode 114 is a portion of a memory cell. This means that the spaces between spacers 110 are formed before the second gate electrode 114 and thus before the memory cells. Further, there is no indication in Lee et al. of forming source and drain select gates before forming a source slot and a drain contact region, or of forming a portion of a drain contact region directly over a drain select gate. In fact, Lee et al. does not teach the formation of any slots or regions relative to source and drain select gates. Therefore, Lee et al. does not include each and every recitation of claim 1, so claim 1 should be allowed.

Claims 2-8 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Therefore, claims 2-8 should be allowed.

Claim 9 recites that a dielectric layer is formed on a substrate, a NAND string disposed on the substrate, and source and drain select gates respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, the NAND string comprising a plurality of memory cells connected in series, and that a bulk insulation layer is formed on the dielectric layer. This means that the dielectric layer is formed after the NAND string of memory cells and the source and drain select gates, and that the bulk insulation layer is

formed after the dielectric layer. There is no indication of this in Lee et al. Claim 9 further recites that a source slot and a drain contact region are formed in the bulk insulation layer respectively adjacent the source select gate and the drain select gate using a single mask disposed on the bulk insulation layer, where a portion of the drain contact region directly overlies the drain select gate. There is no indication in Lee et al. of forming a source slot and a drain contact region in a bulk insulation layer that is formed on dielectric layer that is formed on a NAND string of memory cells and source and drain select gates after the formation of the NAND string of memory cells and the source and drain select gates. Further, there is no indication in Lee et al. of forming a portion of a drain contact region directly over a drain select gate. In fact, Lee et al. does not teach the formation of any slots or regions relative to source and drain select gates. Therefore, Lee et al. does not include each and every recitation of claim 9, so claim 9 should be allowed.

Claims 10-13 and 17 depend from claim 9 and are thus allowable for at least the same reasons as claim 9. Therefore, claims 10-13 and 17 should be allowed.

Claim Rejections Under 35 U.S.C. § 103

Claims 14-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,846,863). Claims 18-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,846,863) in view of Sakui et al. (U.S. Patent No. 6,411,548). Applicant respectfully traverses.

Claim 9 is patentably distinct from Lee et al. The taking of Official Notice that Lee et al. discloses the claimed invention except for selecting a specific material for the dielectric layer and bulk insulation layer fails to overcome the deficiencies of Lee et al. with respect to claim 9. Claims 14-16 depend from claim 9 and are thus allowable for at least the same reasons as claim 9. Therefore, claims 14-16 should be allowed.

Claims 18 and 25 each recite the following: "forming a bulk insulation layer on the dielectric layer; forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate, wherein a portion of the drain contact region directly overlies the drain select gate; and removing the dielectric layer from the substrate within the source slot and drain contact region to expose the substrate. Claim 18 also

recites: "forming a source line in the source slot and a drain contact in the drain contact region; and forming a bit line contact in contact with the drain contact." Claim 25 further recites: forming a polysilicon plug in the source slot in contact with the substrate and a polysilicon plug in the drain contact region in contact with the substrate; forming an electrically conducting plug on the polysilicon plug in the source slot and on the polysilicon plug in the drain contact region; and forming a bit line contact through an interlayer dielectric on the bulk insulation layer in contact with the electrically conducting plug in the drain contact region. The Examiner admits that Lee et al. does not include this.

Moreover, Sakui et al. includes a contact hole 30d (Figure 12) reaching the drain region 28d. No portion of contact hole 30d is formed directly overlying gate electrode (or select gate line) 27(SSL). In Figure 44, a contact plug 31d is formed in the contact hole 30d and is connected to an intermediate layer 33d that is connected to bit line 36(BL) through a contact plug 32d. Sakui et al. also includes a source line 33(SL) connected to a contact plug 31s formed in a contact hole 30s. However, formation of intermediate layer 33d requires a different step than the formation of contact plugs 31s and 31d. This means that Sakui et al. does not form contact holes 30s and 30d and a region directly overlying gate electrode (or select gate line) 27(SSL) using a single mask layer. Therefore, Sakui et al. does not recite or suggest each and every element of claim 18 or 25. Moreover, there is no indication Sakui et al. that there is anything wrong the method of Sakui et al., so there is no motivation for changing the of Sakui et al. This means that Lee et al. in combination with Sakui et al. fails to overcome the deficiencies of Lee et al. with respect to claims 18 and 25, so claims 18 and 25 should be allowed.

Claims 19-24 depend from claim 18 and are thus allowable for at least the same reasons as claim 18. Claims 26-28 depend from claim 25 and are thus allowable for at least the same reasons as claim 25. Therefore, claims 19-24 and 26-28 should be allowed.

Allowable Subject Matter

Applicant acknowledges that claims 42-62 were allowed.

CONCLUSION

In view of the above remarks, Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

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